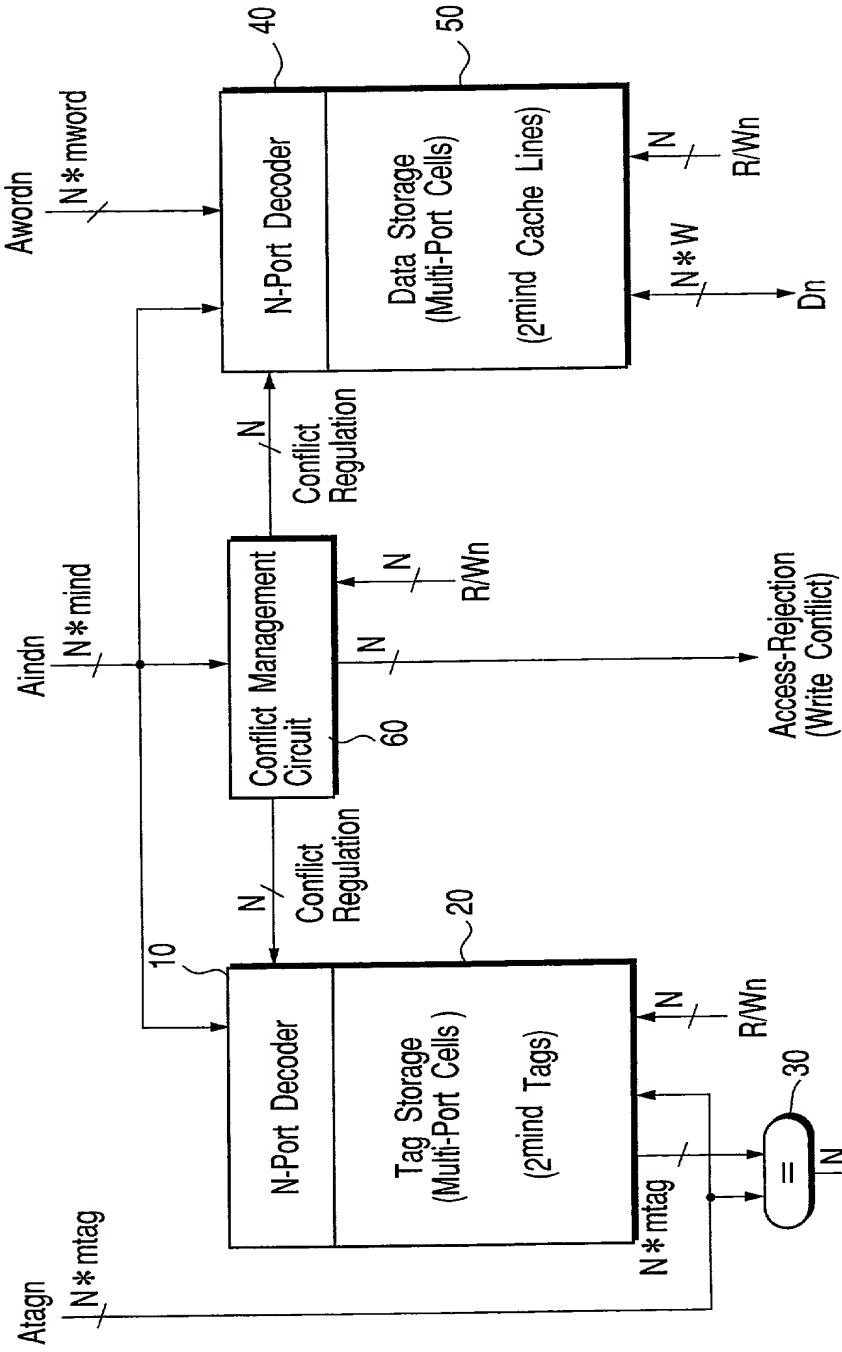

FIG. 1 PRIOR ART

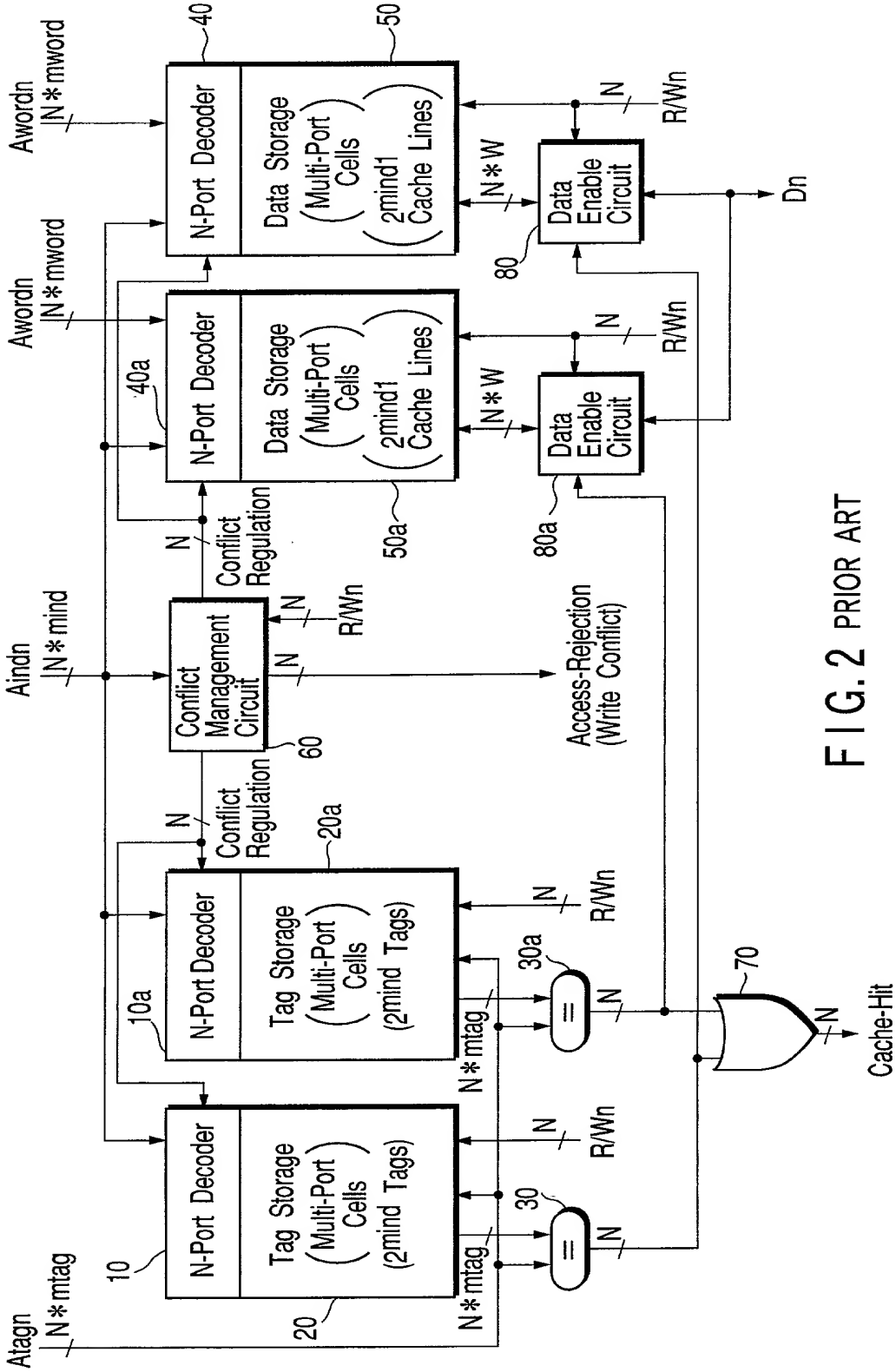

FIG. 2 PRIOR ART

Atag (mtag bits)	Aind (mind bits)	Aword (mword bits)	Abyte (mbyte bits)

FIG. 3 PRIOR ART

General Case

Atag (mtag bits)	Aind2 (mind2 bits)	Aind1 (mind1 bits)	Aword (mword bits)	Abyte (mbyte bits)

FIG. 5A

512Kbit, Direct-Mapped, 8-Port Cache, 4 Word Per Line Cache Memory
(32Bit Addresss Space, 32bit Wordlength)

	Atag (bits)	Aind2 (bits)	Aind1 (bits)	Aword (bits)	Abyte (bits)
Conventinal Multi-Port Cache Memory	16	12		2	2
Multi-Port Cache Memory according to the invention	16	7 Data-Storage: 128 blocks each 4Kbit Tag-storage: 128 blocks each 480bit	5	2	2

FIG. 5B

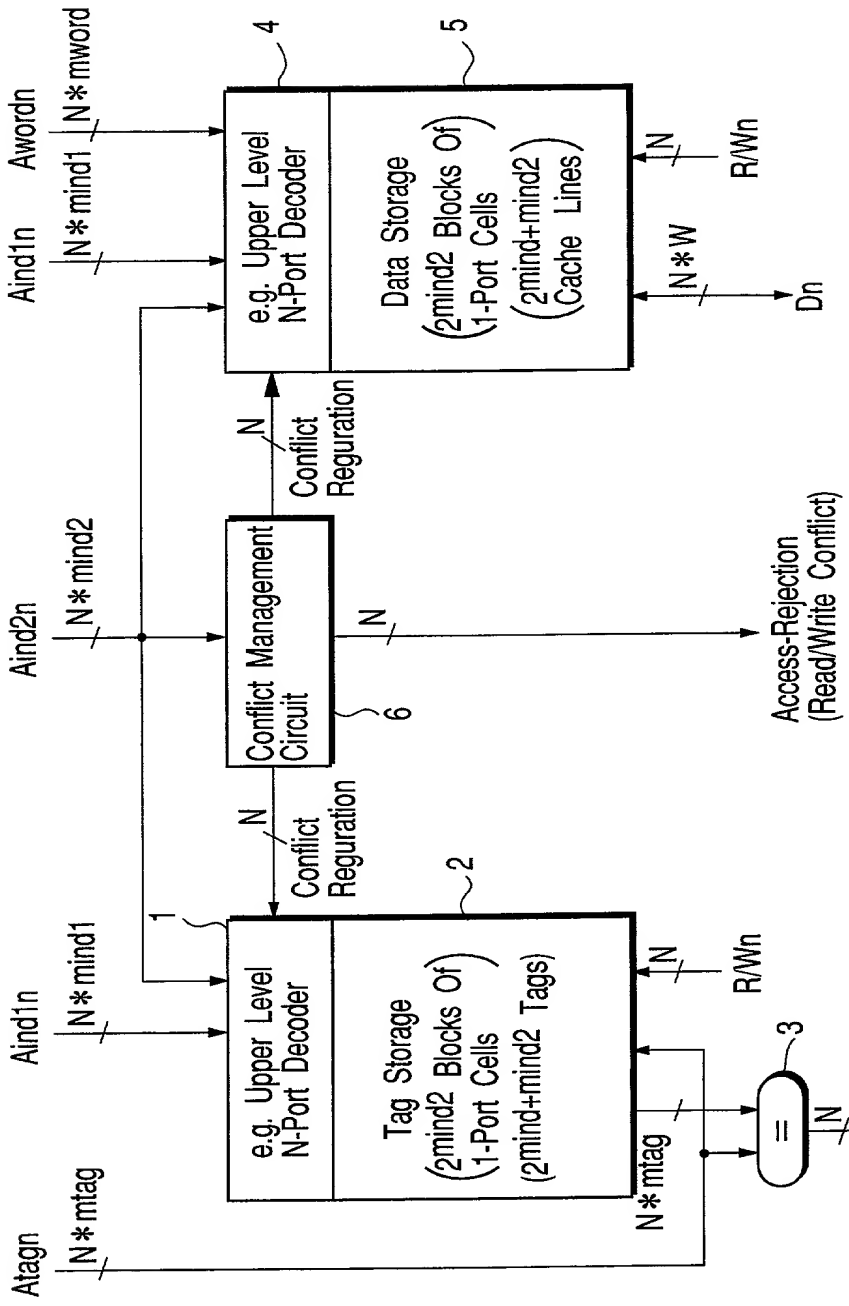
Awordn
N*mword
Aind1n
N*mind1
4
5
e.g. Upper Level N-Port Decoder
Data Storage (2mind2 Blocks Of 1-Port Cells (2mind+mind2 Cache Lines)
N
R/Wn
N*W
Dn
N
Conflict Regruration
Aind2n
N*mind2
Conflict Management Circuit
6
N
Access-Rejection (Read/Write Conflict)
N
Conflict Regruration
1
2
Aind1n
N*mind1
e.g. Upper Level N-Port Decoder
Tag Storage (2mind2 Blocks Of 1-Port Cells (2mind+mind2 Tags)
N
R/Wn
3
=
N
Cache-Hit
Atagn
N*mtag
N*mtag

FIG. 4

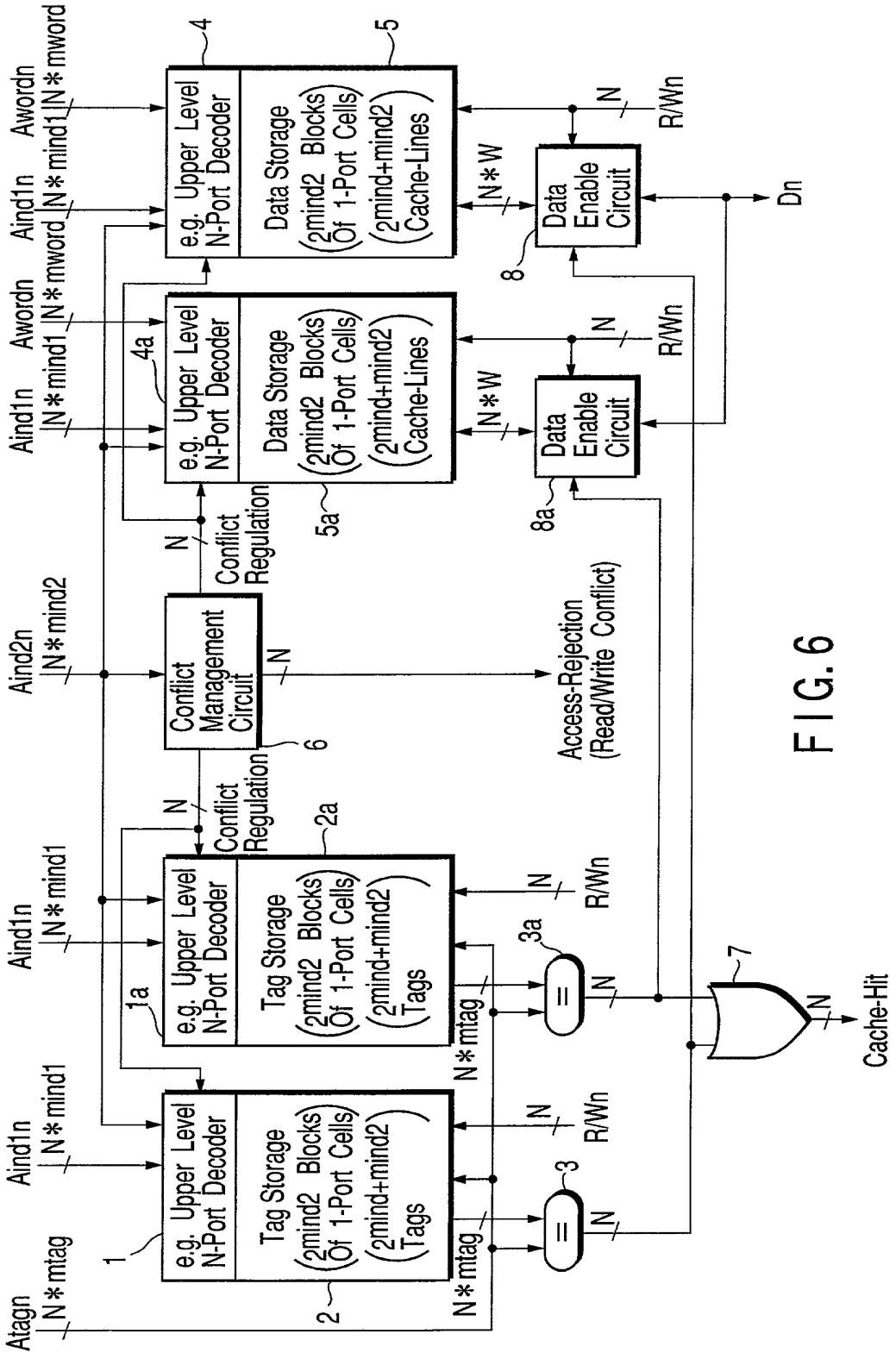
Aind1n
N*mind1
Awordn
N*mind1
N*mword
Aind2n
N*mind2
Atagn
N*mtag
e.g. Upper Level N-Port Decoder
Tag Storage (2mind2 Blocks Of 1-Port Cells) (2mind+mind2 Tags)
Data Storage (2mind2 Blocks Of 1-Port Cells) (2mind+mind2 Cache-Lines)
Conflict Management Circuit
Conflict Regulation
Data Enable Circuit
N*W
N*mtag
R/Wn
Dn
Access-Rejection (Read/Write Conflict)
Cache-Hit
1
1a
2
2a
3
3a
4
4a
5
5a
6
7
8
8a

FIG. 6

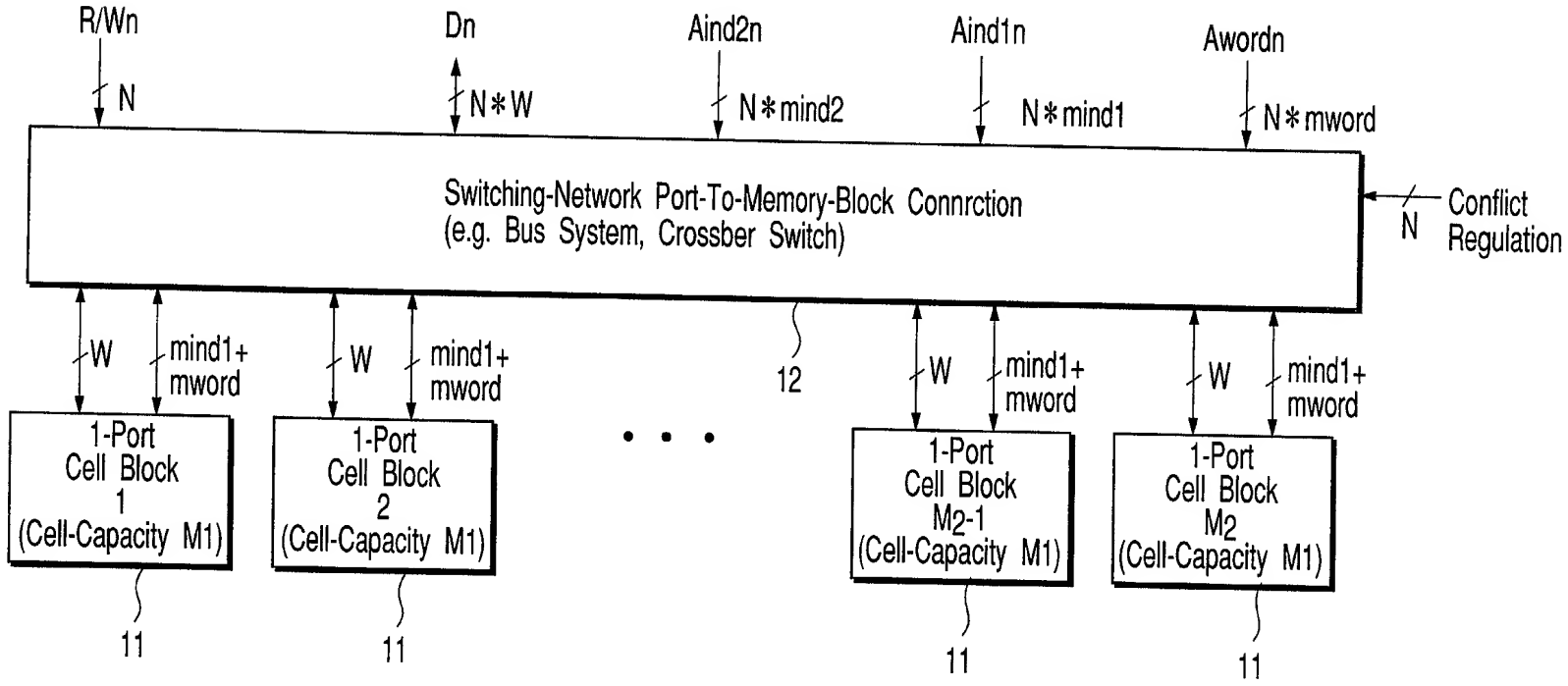

FIG. 7

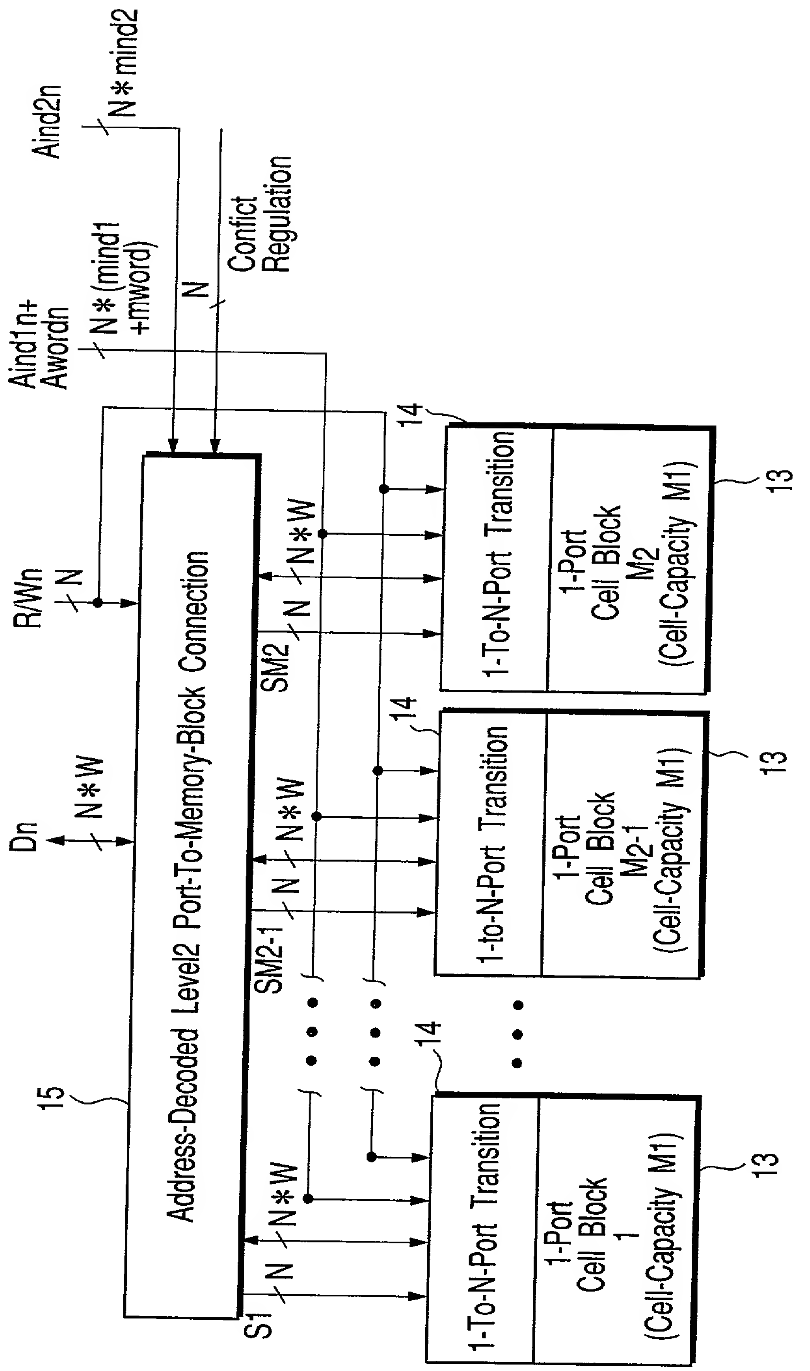
Aind2n
N∗mind2
Aind1n+
Awordn
N∗(mind1
+mword)
N
Conflct
Regulation
R/Wn
N
Dn
N∗W
15
Address-Decoded Level2 Port-To-Memory-Block Connection
SM2
N
N∗W
SM2-1
N
N∗W
S1
N
N∗W
14
1-To-N-Port Transition
1-Port
Cell Block
M2
(Cell-Capacity M1)
13
14
1-to-N-Port Transition
1-Port
Cell Block
M2-1
(Cell-Capacity M1)
13
14
1-To-N-Port Transition
1-Port
Cell Block
1
(Cell-Capacity M1)
13

FIG. 8

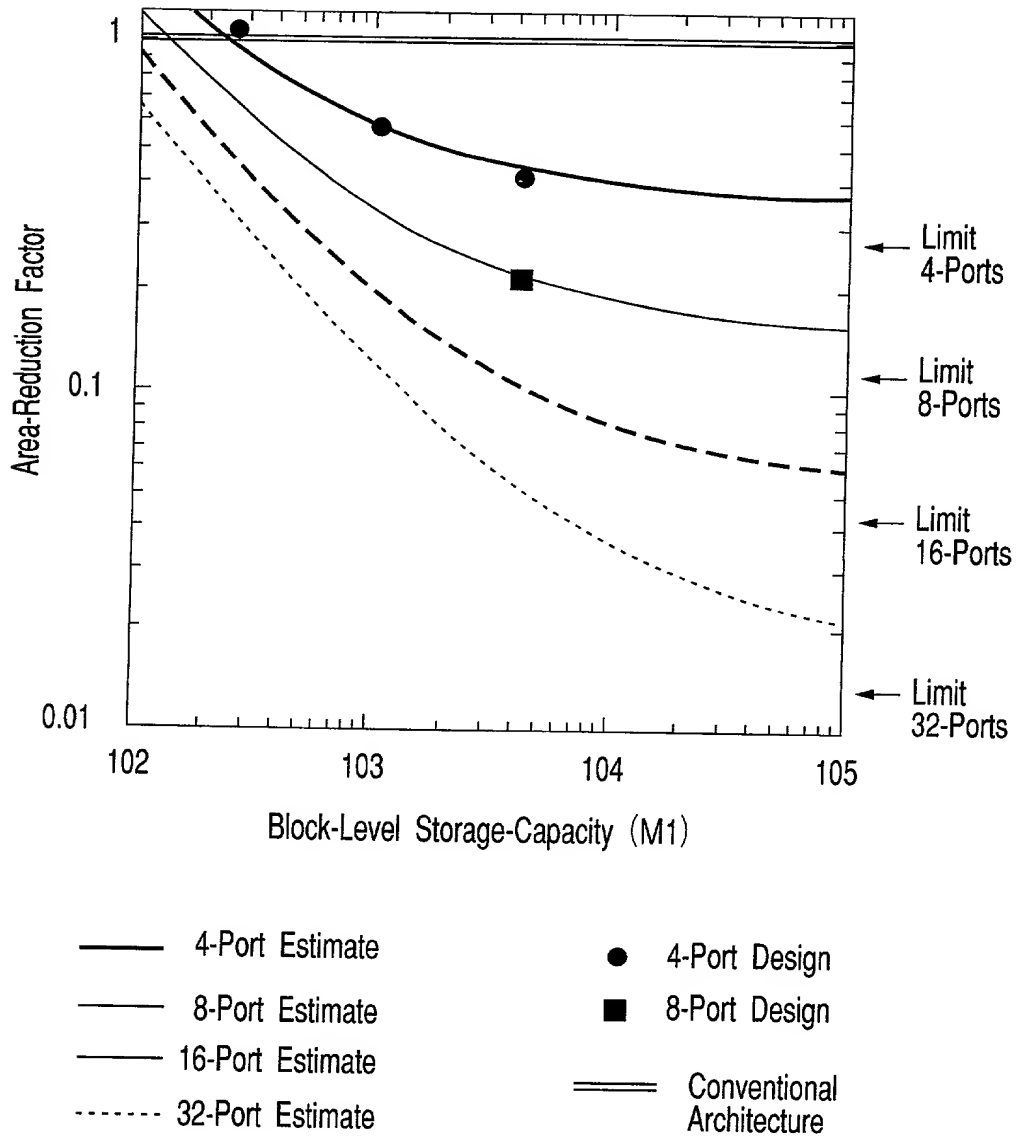
1
0.1
0.01
Area-Reduction Factor
102
103
104
105
Block-Level Storage-Capacity (M1)
Limit 4-Ports
Limit 8-Ports
Limit 16-Ports
Limit 32-Ports
4-Port Estimate
8-Port Estimate
16-Port Estimate
32-Port Estimate
4-Port Design
8-Port Design
Conventional Architecture

FIG. 9

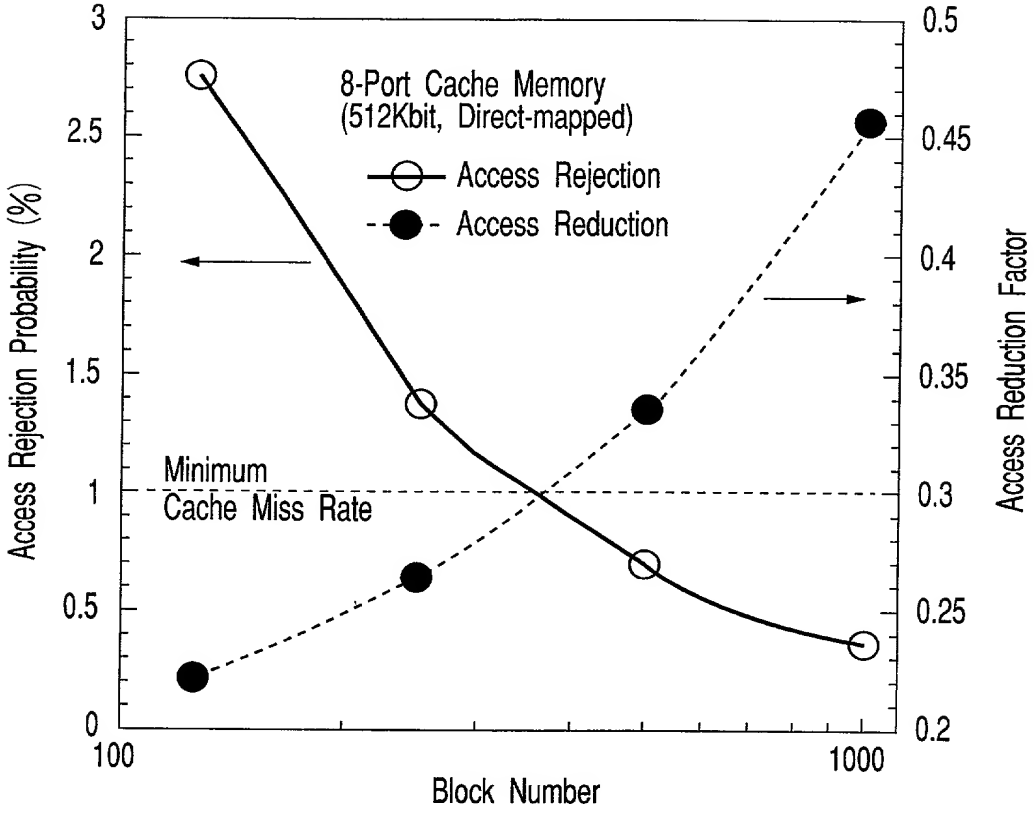
8-Port Cache Memory
(512Kbit, Direct-mapped)
Access Rejection
Access Reduction
Minimum
Cache Miss Rate
Access Rejection Probability (%)
Access Reduction Factor
Block Number
3
2.5
2
1.5
1
0.5
0
0.5
0.45
0.4
0.35
0.3
0.25
0.2
100
1000

FIG. 10